

**Amendments to the Specification:**

Please replace the paragraph of the application commencing at line 3 of page 27 with the following amended paragraph:

Turning back to level adapter 543, each coefficient  $H(n)$ , in accordance with equations 5 and 4, is a  $6 \times 1$  matrix in which each of the six individual values comprising  $H(n)$ , i.e.,  $h_0(n)$ ,  $h_1(n)$ , ...,  $h_5(n)$ , represent the levels of six consecutive sample slots in the echo signal. During training, the error signal,  $e(n)$ , includes the effect of the robbed bit. Any sample slots within that group of six consecutive slots that contain a robbed bit will have a particular amplitude which will be different than the amplitude of those sample slots which do not contain a robbed bit. Accordingly,  $H(n)$  discloses the locations of robbed bits in the echo. Therefore, the values  $H(n)$  are also provided to the robbed bit detector block 537. The robbed bit detector ~~block 534~~ block 537 can be a simple combinational logic circuit that determines from  $H(n)$  the sample slots that contain robbed bits and informs the robbed bit generator 511 of the locations of the robbed bits via signal line 551.